An Alignment Insensitive Separable Electromagnetic Coupler for High Speed Digital Multidrop Bus Applications

J. R. Benham†, R. Amirtharajah, J. Critchlow†, T. Simon, T. F. Knight, Jr‡

†Intel Desktop Platform Architecture Group, Hudson, MA 01749, USA
‡MIT Artificial Intelligence Laboratory, Cambridge, MA 02139, USA

Abstract — **A separable electromagnetic coupler was designed, simulated, fabricated, and tested as part of a prototype eight module multidrop memory bus running at 1.6 Gb/s per differential pair. The coupler consists of broadside coupled traces, one on a rigid motherboard and the other on a flex circuit soldered to a daughter card. The zigzag geometry of the traces reduces variation in coupling coefficient due to horizontal and vertical misalignment of the coupler halves. Simulation and testing indicates that a target capacitive coupling coefficient of 0.34, which has been selected to balance signal transmission level requirements against motherboard impedance discontinuity effects, can be achieved with little variation over +/- 12 mil alignment tolerance.**

I. INTRODUCTION

Figure 1 shows a system level block diagram of the prototype memory system and highlights the use of AC coupling [1,2,3]. A memory controller communicates with up to eight cards on a multidrop bus. All signaling is differential and parallel terminated at both ends on the motherboard and the cards (discrete resistors at far ends, calibrated on chip transistor termination at near ends). The AC transmission line coupling, targeted in a light coupling range ($0.27<K_c<0.43$), minimizes intersymbol interference (ISI) by maintaining impedance continuity along the bus and isolating the bus from on-card parasitics. The coupling range meets a dual constraint: not too large for ISI (for example reflection coefficients between -0.15 and -0.18 at coupled to uncoupled interfaces along the bus), and not too small for received amplitudes (worst case 120 mV received with Vdd=2.5 volts). The AC coupling is bilaterally symmetric, so the signals and I/O circuits in both directions are the same.

II. COUPLER DESIGN

The signal integrity benefits of achieving a selected range of coupling performance can be illustrated by considering the case of a lossless coupler embedded in a homogeneous dielectric, and where the propagation is essentially TEM. The relationship between K_c and the reflection coefficient at the coupler can then be deduced as illustrated in Figure 2. The corresponding relationship between K_c and the transmission coefficient (transmission loss) to the 8th coupler is shown in Figure 3.

From this simplified analysis it is shown that the selected K_c range ($0.27<K_c<0.34$) results in a worst case reflection coefficient range of 0.15 - 0.18, and that the corresponding signal transmission coefficient (signal attenuation) at the 8th coupler on the bus line is 0.3 – 0.4. In reality, adjustment of the differential transmission line geometry in the feed and inter-coupler regions can be used to further minimize the impedance discontinuities resulting from the presence of the couplers on the transmission bus.

The coupling is achieved with backward crosstalk between closely spaced traces. In the test system, the coupled traces broadside couple to the motherboard bus microstrip lines. To implement a separable connector, the coupled traces are microstrip lines on a bent loop of standard 2 metal layer flex soldered at both ends to the bottom of rigid PC board DIMMs that carry DRAMs and a buffer chip. The flex circuit was designed using off-the-shelf 0.5 and 2.0 mil thick polyimide film materials and manufactured using conventional lamination techniques. A socket mounted on the motherboard guides the card and flex assembly down during insertion, pressing the flex loop flat against the motherboard (see Figure 4). Trace geometries are chosen to provide 50 ohm impedances and the desired coupling in a standard FR4, four-layer PC motherboard. Flex geometries meet coupling and impedance targets while allowing mechanical flexibility and durability. A vertical pin attached to the bottom of the DIMM passes through holes in the flex and motherboard for alignment of coupled traces to +/-12 mils.

The design of couplers for this application was primarily constrained by the accuracy with which the flex circuit and motherboard conductors can be aligned using large volume, low cost manufacturing techniques. To this end, zigzag geometries [4] of both motherboard

0-7803-7695-1/03/$17.00 © 2003 IEEE

and flex traces provide coupling strength robustness against residual positional misalignment by stabilizing overlap area and increasing fringing field contribution (see Figure 5).

During development of the coupler it was determined that a key feature of the design was that the angular rotation of the conductor segments about the longitudinal axis in conjunction with the number of zigzag segments could be used to determine the stability of the coupling performance over a given range of X and Y axis misalignment. In general terms, larger angular rotations between consecutive conductor segments were shown to produce greater performance stability in return for a reduction in potential coupling efficiency and directivity. Further while it is possible to configure both differential signal conductor pairs with corresponding segments parallel or non-parallel, it was established that the non-parallel structure maintains better coupling symmetry in the presence of X,Y axis misalignment.

The width of the coupled pulse, and therefore the energy content of the pulse delivered at the receiving device is dependant on the physical length of the coupled structure. A minimum length coupler design is generally desirable for high circuit density and minimal inter- and intrasymbol interference. However the need to achieve an adequate bit error rate at the receiver without violating transistor performance limitations places a minimum energy transfer constraint on the coupler design. The system design discussed here utilized a full custom differential receiver circuit in an off the shelf 0.25 um silicon CMOS logic process, and it was determined by simulation that a 1 cm. coupler length would provide an adequate level of coupled pulse power at the receiver input. Later analysis of the measured waveforms showed that each coupled load extracted less than 0.1 percent of the incident signal power in this regime. As the gain-bandwidth product of future CMOS devices increases, it will be possible to use shorter couplers and lower levels of coupled power as long as bit error rate requirements are met.

The minimum length constraints require the coupler performance to lie between two physical regimes. The coupler must be sufficiently long to provide some distributed line behavior; otherwise it behaves as a lumped capacitance with a corresponding impedance discontinuity. On the other hand, circuit density needs at these data rates and signal frequencies require that it be too short to behave as a traditional quarter-wavelength directional coupler [5]. However, the coupler length must scale (decrease) as frequencies increase to avoid having multiple symbols simultaneously coupling through to the receiver and interfering with each other. This scaling requirement dovetails nicely with the continued need to increase circuit density and integration of digital systems.

III. Simulation and Modeling

The performance of the coupler was extensively modeled using both Ansoft Q3D and Ansoft HFSS tools to obtain the microwave scattering performance and equivalent electrical parameters. An analysis of the coupler behavior was performed over the anticipated manufacturing spread of dielectric and conductor dimensions and dielectric properties of the materials. The computed variation in K_c with conductor misalignment is shown for the weakest, median and strongest coupling scenarios in Figure 6. The 3D computer model of Figure 7 also incorporates the performance degradation due to the presence of air gaps resulting from the non-planarity of the motherboard surface and adhesive squeeze-out in the flex-circuit as shown in the simplified cross-section of Figure 8.

The computed Scattering parameters in Figure 9 demonstrate that the coupling and reflection coefficient goals were met in the frequency range of interest. Because of the minimal length and the mixed-dielectric nature of the coupler, the directivity is about 6 dB for the relevant frequencies.

IV. Test Results

The prototype coupler was fabricated using a two component connector type mechanical assembly shown in Figure 10. A clamping mechanism mounted to the daughter card provides mechanical retention for the ends of the flex-circuit and strain relief for the coupler conductors that are flow soldered to contact pads on the daughter card edge. A second retention structure mounted on the motherboard ensures proper insertion of the daughter card. The test couplers occupy 400 x 42 mils. Including the zigzagging lengths, incident signal edges induce coupled pulses of 400 ps width.

Figure 11 shows a simulated coupled waveform compared to a measured waveform for a pulse propagating on the motherboard trace and received through the coupler at an oscilloscope.

V. Summary

Generally good agreement was achieved between computed and measured coupler performance and waveforms (within 20% in the worst case). 1.6 Gbps per differential pair performance was demonstrated in an 8 load prototype memory bus based on the coupler design.

Multiple memory read and write transactions were executed continuously on the bus for over four weeks without observing a bit error. From these measurements, we estimate that the memory bus BER was < 2.0e-17.

REFERENCES

[1] Simon, T. et al., "A 1.6 Gb/s/pair Electromagnetically Coupled Multidrop Bus Using Modulated Signaling", ISSCC 2003, Feb. 2003, pp. 184-5, 487.

[2] Simon, T. et al., "Electromagnetically-Coupled Bus System," US Pat. App. No. 09/714,321 (2000).

[3] Osaka, H. et al., "Fast Data Transfer Bus," US Pat. no. 5,638,402 (1997).

[4] Benham, J., Marketkar, N., and Amirtharajah, R., "An Electromagnetic Coupler," US Pat. App. No. 09/714.899 (2000).

[5] Pozar, D., *Microwave Engineering*, John Wiley & Sons, Inc., New York, 2nd edition, 1998.

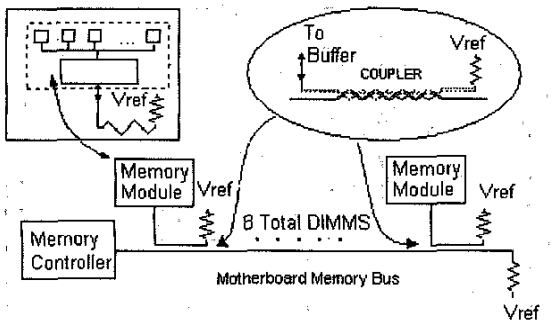

Fig. 1. System Block Diagram

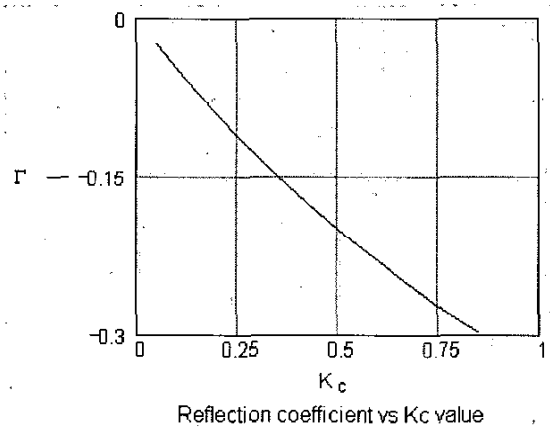

Fig. 2. Reflection coefficient vs. K_c

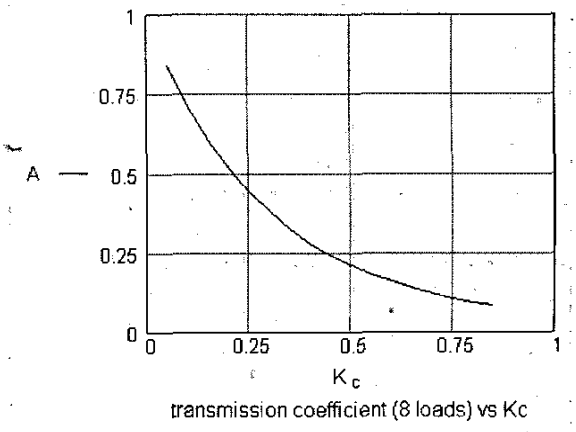

Fig. 3. Transmission coefficient vs. K_c

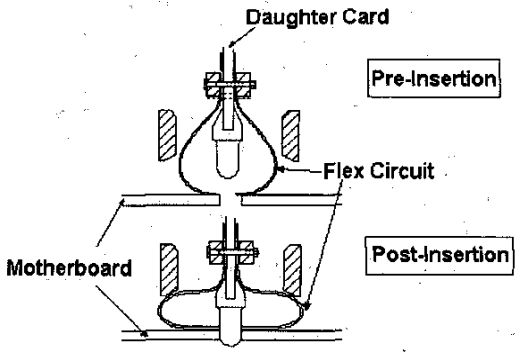

Fig. 4. Coupler-Motherboard Interface

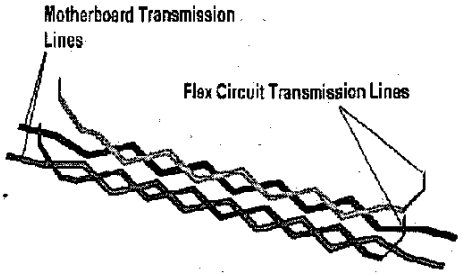

Fig. 5. Coupler Zig-Zag Geometry

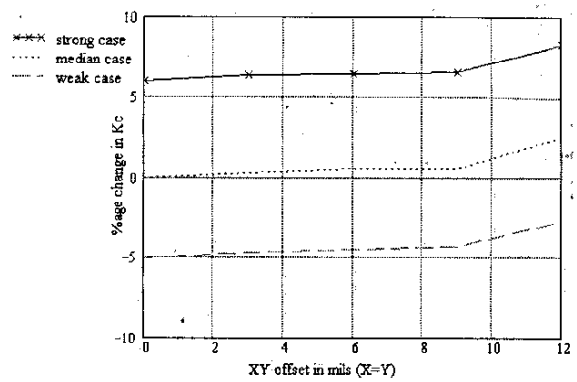

Fig. 6. Percentage K_c Variation vs. X and Y Axis Offset

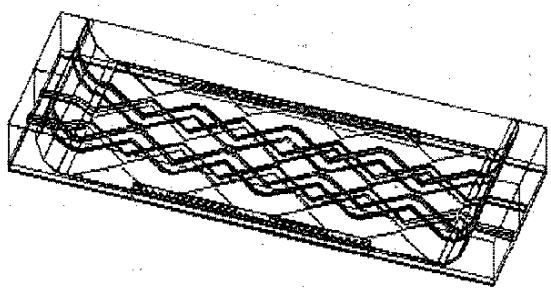

Fig. 7. Ansoft HFSS 3D Model of Installed Coupler

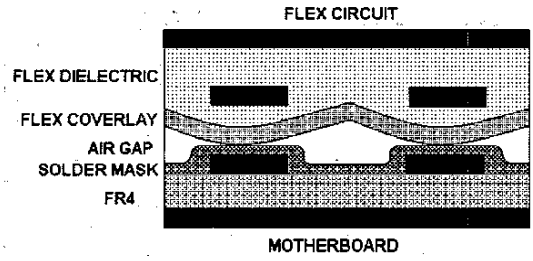

Fig. 8. Simplified Coupler Cross-Section

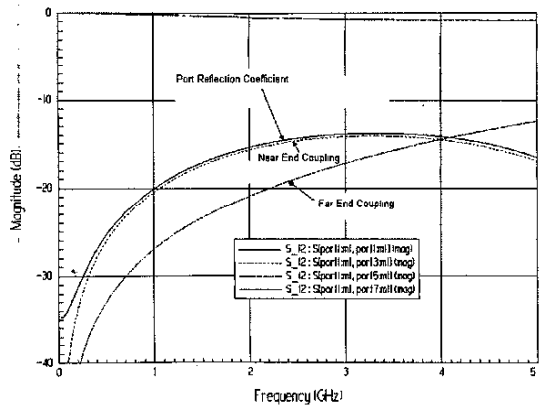

Fig. 9. Computed Scattering Parameters

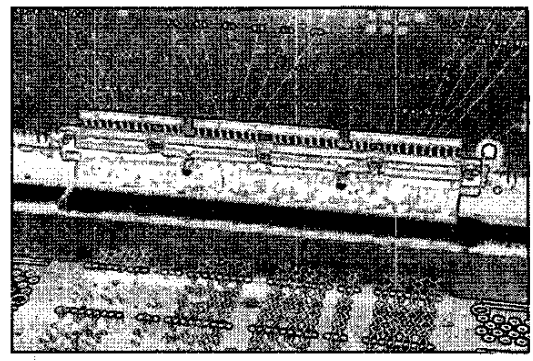

Fig. 10. Coupler Installation

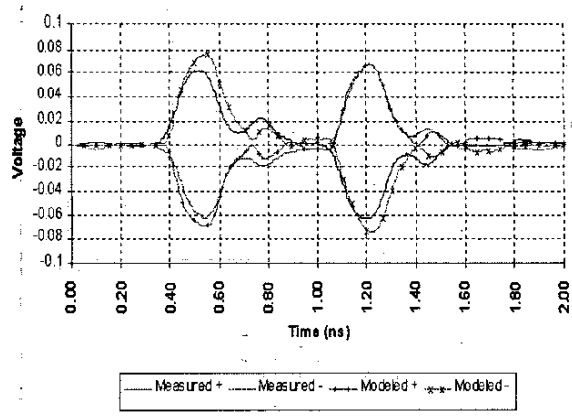

Fig. 11. Computed vs. Measured Differential Waveform